CLEAN DATA STROBE SIGNAL GENERATING CIRCUIT IN READ INTERFACE DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] A claim for the benefit of priority under 35 U. S. C. §119 is made to Korean Patent Application No. 10-2015-0144835, filed Oct. 16, 2015 in the Korean Intellectual Property Office (KIPO), the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] The inventive concepts described herein relate to a memory system, and more particularly, to an interface device which interfaces information between a semiconductor memory device and a memory controller.

[0003] The need for low-power and high-density memories are increasing to improve the performance of electronic systems.

[0004] For implementation of the low-power and high-density memories, a high bandwidth memory is receiving attention to provide high performance in situations such as low-power high-speed operation.

[0005] An LPDDR (Low Power Double Data Rate) type of Dynamic Random Access Memory (DRAM) mounted in a mobile device is a semiconductor memory device that operates at a low-power double data rate. The semiconductor memory device can be controlled by a memory controller communicating with a processor or System on Chip (SoC). In read operation mode, the memory controller receives read data using a data strobe signal.

[0006] When a ground termination type of on-die termination operation is performed in a differential receiver of an interface device and a data strobe signal is not provided from a semiconductor memory device, a dirty signal of tri-state condition may be outputted from the differential receiver.

SUMMARY

[0007] Various example embodiments of the inventive concepts provide a clean data strobe signal generating circuit in a read interface device, which can generate a clean data strobe signal without a delay control circuit or without performing a training operation.

[0008] Various example embodiments of the inventive concepts also provide a clean data strobe signal generating circuit in a read interface device, which can generate a clean data strobe signal by masking a data strobe signal, generated in asynchronization with an internal clock of an interface device, without gate signal training.

[0009] One aspect of some example embodiments of the inventive concepts is directed to provide a clean data strobe signal generating circuit in a read interface device. The clean data strobe signal generating circuit may include a first receiver configured to receive a differential data strobe signal comprising at least a first input data strobe signal and a second input data strobe signal, and output a first single ended data strobe signal, a second receiver configured to receive the second input data strobe signal and a reference voltage signal, and based on the received second input data strobe signal and the reference voltage signal, output a second single ended data strobe signal, a gate signal generator configured to generate a data strobe gate signal synchronized with the first single ended data strobe signal based on the first and second single ended data strobe signals and a memory gate signal, the memory gate signal including a pulse width that varies in accordance with a burst length after termination of a read latency, at least one logic gate configured to receive the first single ended data strobe signal and the data strobe gate signal to generate a clean data strobe signal for receiving read data.

[0010] The differential data strobe signal may be transmitted from a semiconductor memory device.

[0011] The phase of the second single ended data strobe signal may be opposite to the phase of the first single ended data strobe signal except in an unknown section of the first single ended data strobe signal.

[0012] The data strobe gate signal may transition to a first level in response to a signal synchronized with the second single ended data strobe signal, the number of toggles of the first single ended data strobe signal may be counted in response to a count start signal synchronized with a first falling edge of the first single ended data strobe signal, and the data strobe gate signal may transition to a second level in response to a reset signal generated after the counting of the number of toggles.

[0013] When the first single ended data strobe signal is inverted by an inverter, the at least one logic gate may be a NOR gate that generates a NOR response as the gating response.

[0014] The differential data strobe signal may be applied from an LPDDR4 DRAM device configured to perform a ground voltage termination type of on-die termination operation.

[0015] The clean data strobe signal may be provided as a data clock signal of a First-In First-Out (FIFO) memory device configured to receive the read data.

[0016] The pulse width of the memory gate signal may be half the pulse width of the burst length.

[0017] A pulse window of the data strobe gate signal when an extra toggling exists in the first single ended data strobe signal may become narrower than a pulse window of the data strobe gate signal when the extra toggling does not exist.

[0018] Another aspect of some example embodiments of the inventive concepts is directed to provide a clean data strobe signal generating circuit in a read interface device. The clean data strobe signal generating circuit may include a first receiver configured to receive a differential data strobe signal comprising first and second input data strobe signals, and output a first single ended data strobe signal, a second receiver configured to receive the second input data. strobe signal and a reference signal, and based on the received second input data strobe signal and the reference signal, output a second single ended data strobe signal, a memory gate signal generator configured to generate a memory gate signal having a pulse width to which a burst length is applied after termination of a read latency, a gate signal generator configured to receive the first and second single ended data strobe signals and the memory gate signal, and generate a data strobe gate signal by counting a number of toggles of the first single ended data strobe signal based on the memory gate signal, and at least one logic gate configured to receive the first single ended data strobe signal and the data strobe gate signal, and generate a clean data strobe signal for receiving read data, as a gating response.